REMARKS

The application has been amended to place it in condition for allowance at the time of the next Official Action.

The specification is amended to make editorial changes therein.

Claims 25-46 were previously pending in the application. Claims 31, 36, 37, 40, 43 and 46 are canceled, leaving claims 25-30, 32-35, 38, 39, 41, 42, 44 and 45 for consideration.

Applicants note with appreciation the indication that claims 25-30 and 44-45 are allowable. However, applicants note that claims 32-35, 38, 39, 41 and 42 should also be allowable based on their dependence from either claim 25 or 28.

As to the 35 USC §112, second paragraph rejection of claims 25, 28 and 31, the term "characterized" is removed. As to the "adjust feature", claims 25, 28 and 31 are amended to recite "is adjustable so as to adjust a negative resistance value." See, for example, page 10, lines 14-19 wherein a change in inductance is made with respect to a length of the conductor piece. Thus, changing the length of the conductor piece adjusts the inductance and thus the inductance is adjustable.

As to the elements being connected in parallel, please see Figure 11 wherein constant lines 2a and 2b are connected in parallel to a source of the transistor.

As to the recited output terminal, since a negative resistance is obtained by positively feeding back from drain D to gate G of the FET, the output terminal is a terminal unlabeled but noted on the right-hand side of Figure 4 (and Figure 11). See also page 9, lines 4-7. The above changes are believed sufficient to address the 35 USC §112, second paragraph rejection as to claims 25, 28 and 31.

As to claims 26 and 29, these claims are amended to clarify that the signal conductor is for the inductance element (or a capacitance element).

As to claims 41-43, at least Figure 11 shows the output terminal of a negative resistance circuit (far right-hand side of the page) disposed through a distributed constant line 4 connected to the gate of the field effect transistor 1 and that the negative resistance circuit includes a bias voltage power source Vg for supplying the gate G with a predetermined DC voltage, and a resistor (see 9 of Figure 4) connected between the bias power source Vg and said distributed constant line 4 that is connected to the gate G. Accordingly, reconsideration and withdrawal of the 35 USC §112, second paragraph rejection as to claims 41-43 is respectfully requested.

As to claims 44-46, Figure 20 shows a resonator C1, L1, R1 in series with negative resistance circuit R_{N1}. See also page 20, line 20 through page 21, line 9.

In view of the above, it is believed to be apparent that each of the 35 USC §112, second paragraph rejections noted in the Official Action is believed to be addressed and reconsideration and withdrawal of the rejection is respectfully requested.

Canceling claims 31, 36, 37, 43 and 46 is believed to obviate the rejection of claims 31-43 and 46 under 35 USC §103(a) as being unpatentable over Figure 1 of applicants' disclosed prior art in view of SHINO et al. JP 2000-228602.

In view of the present amendment, the foregoing remarks, and by canceling the rejected claims and leaving only claims indicated as allowable or claims that depend therefrom, it is believed that the present application has been placed in condition for allowance. Reconsideration and allowance are respectfully requested.

The Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment or credit any overpayment to Deposit Account No. 25-0120 for any additional fees required under 37 C.F.R. § 1.16 or under 37 C.F.R. § 1.17.

Respectfully submitted,

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